

This cross-sectional diagram illustrates a multi-layered semiconductor device. The bottom layer is labeled 20. Above it are several horizontal layers: 21, 22, 23, 24, 25, 26, 27, 28, and 30. A dashed line A-A' indicates a plane through the middle of the stack. Above the dashed line, there is a layer 31 containing a series of rectangular blocks 32. Above this is another layer 33. The topmost section shows a complex structure with layers 34, 35, 36, 36a, 37, 38, 39, 40, 41, 42, and 43. A dimension L1 is indicated at the top left, and T2 is shown as a thickness parameter. Other labels include F, L2, and various numerical identifiers like 44, 52, 55, 56, and 60.

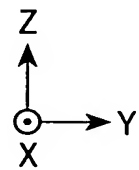


FIG. 1 is a perspective view of a magnetic head assembly. The assembly includes a slider (51) with a front surface (44) facing a recording medium (56). The slider is supported by a suspension (34). A coil (54) is wound around the slider. A coordinate system is shown with Z pointing up, Y pointing right, and X pointing out of the page.

This cross-sectional view shows the device structure along the C-C line. It features a substrate 31 with a top layer 37. A central region contains a stack of layers 39 and 40, with a thickness  $t_1$  indicated. Above this stack is a layer 36, which is divided into regions 36a, 36b, and 36c. A layer 60 is positioned between 36a and 36b. A layer 34 is located above 36c. A layer 35 is on the right side. A layer 42 is on the far right. A layer 41 is between 42 and 40. A layer 38 is between 39 and 35. A layer 33 is at the bottom of the central region. A layer 61 is between 36a and 36b. A layer 31a is on the left side. A layer 39a is between 39 and 40. A layer 40a is between 40 and 36a. A coordinate system is shown at the bottom right with Z pointing up, Y pointing right, and X pointing out of the page.

FIG. 5  
PRIOR ART

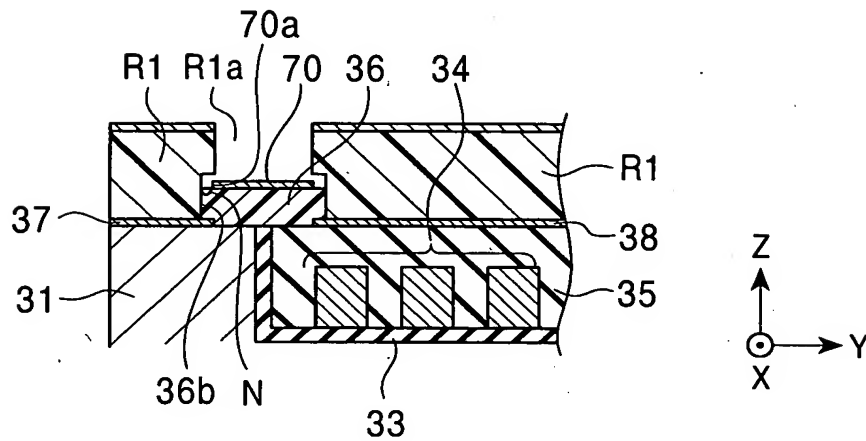
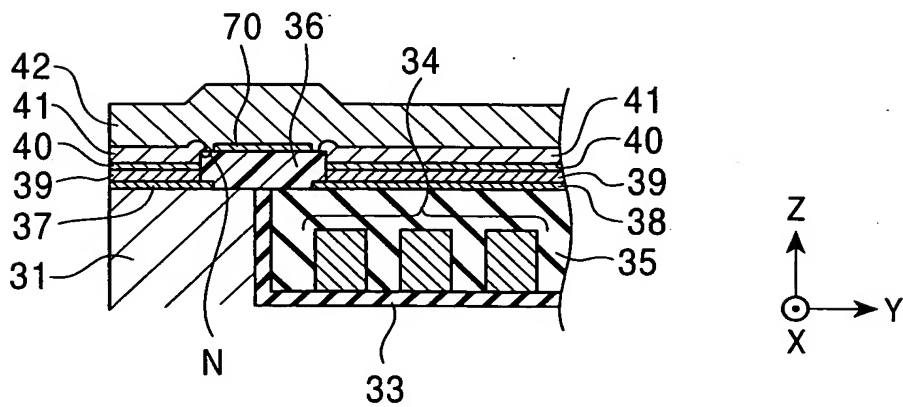


FIG. 6  
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FIG. 7  
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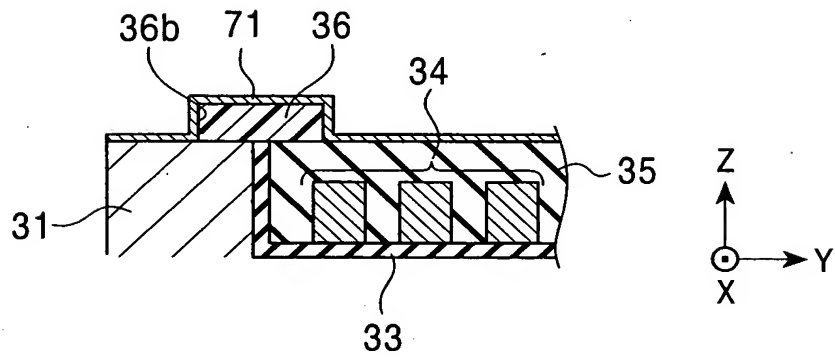


FIG. 8  
PRIOR ART

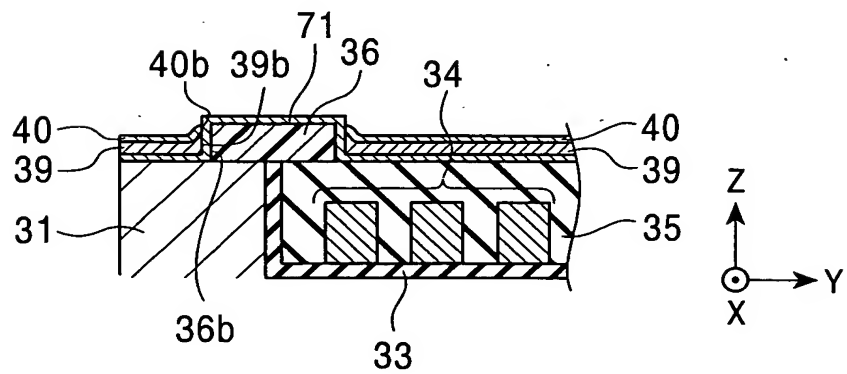
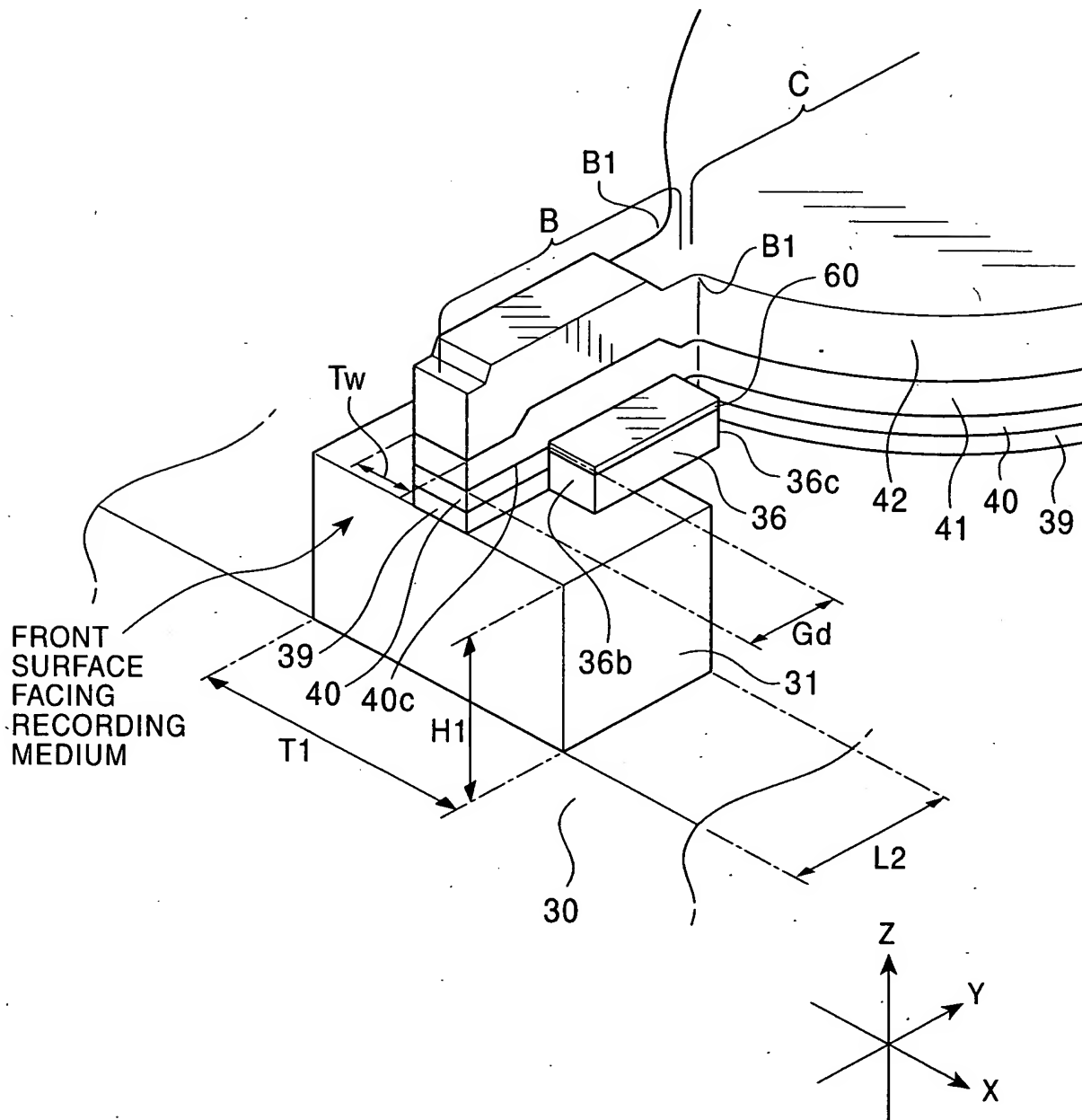


FIG. 9



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FIG. 10

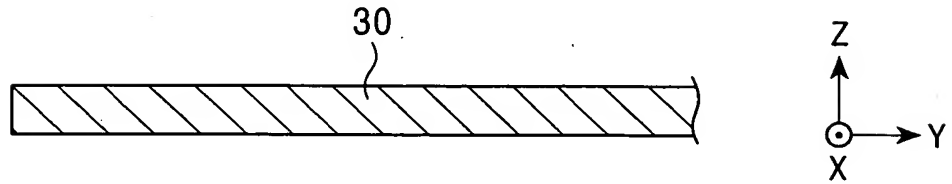


FIG. 11

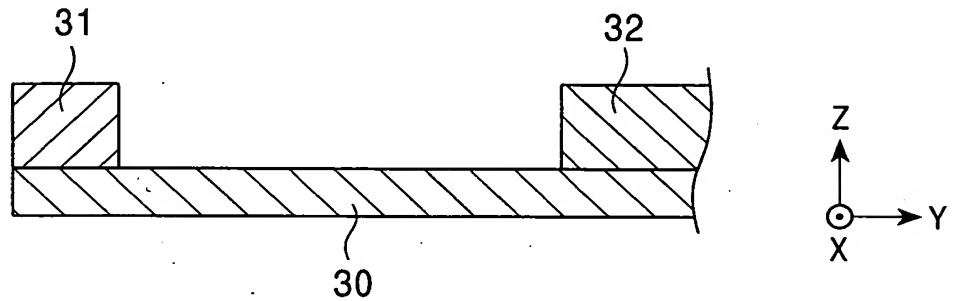


FIG. 12

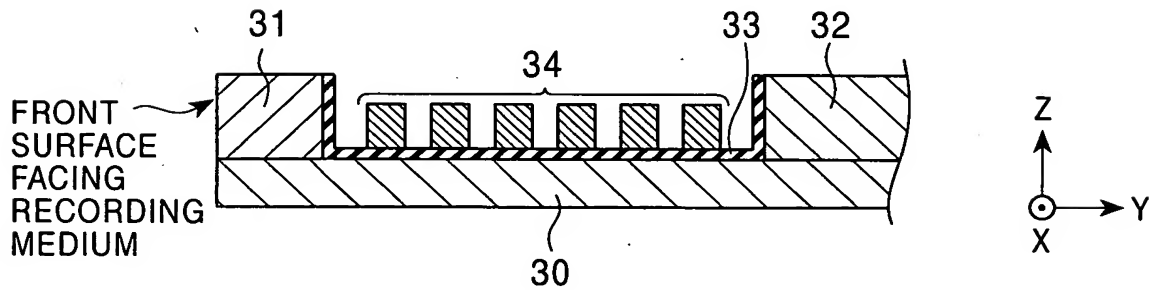
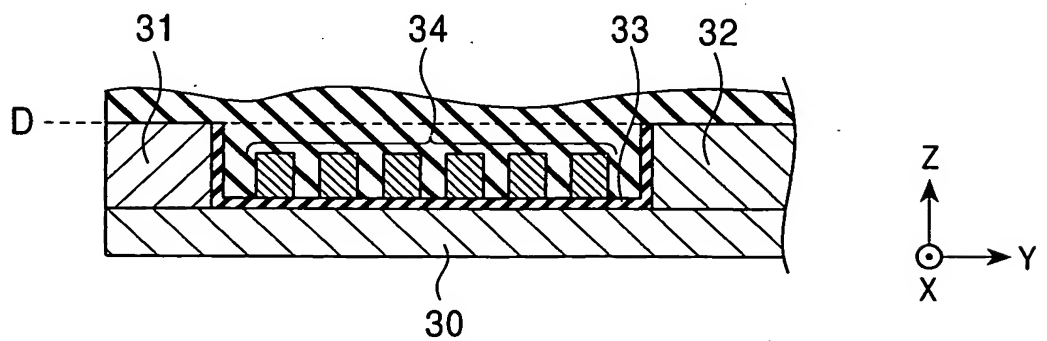


FIG. 13



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FIG. 14

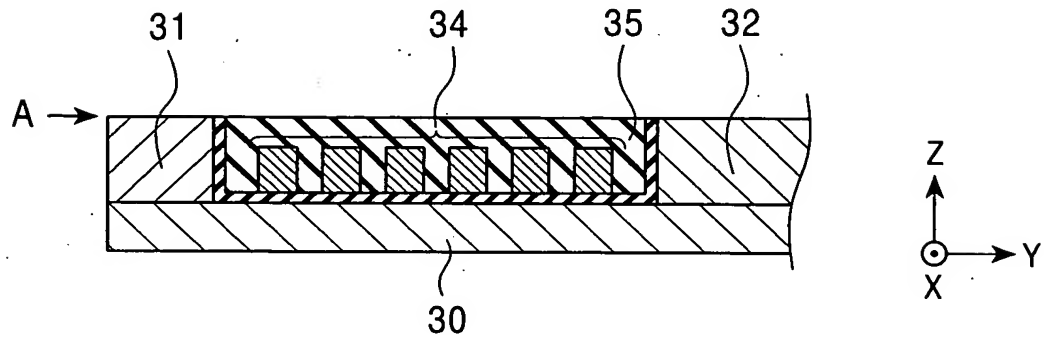


FIG. 15

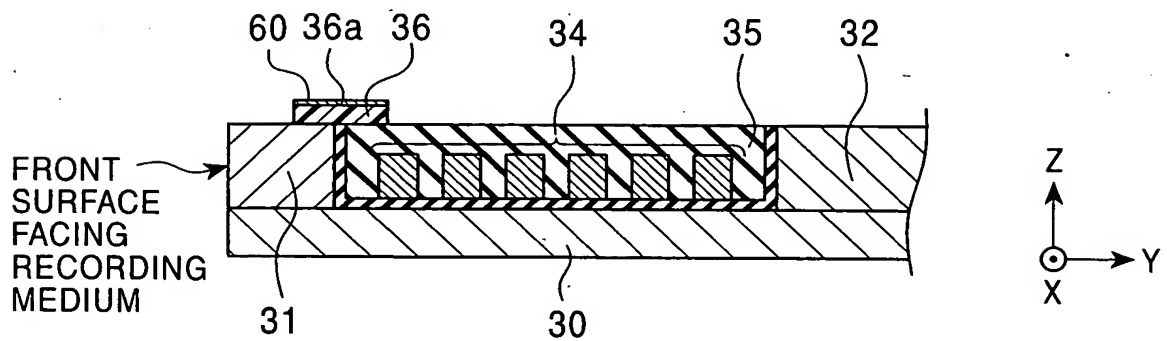


FIG. 16

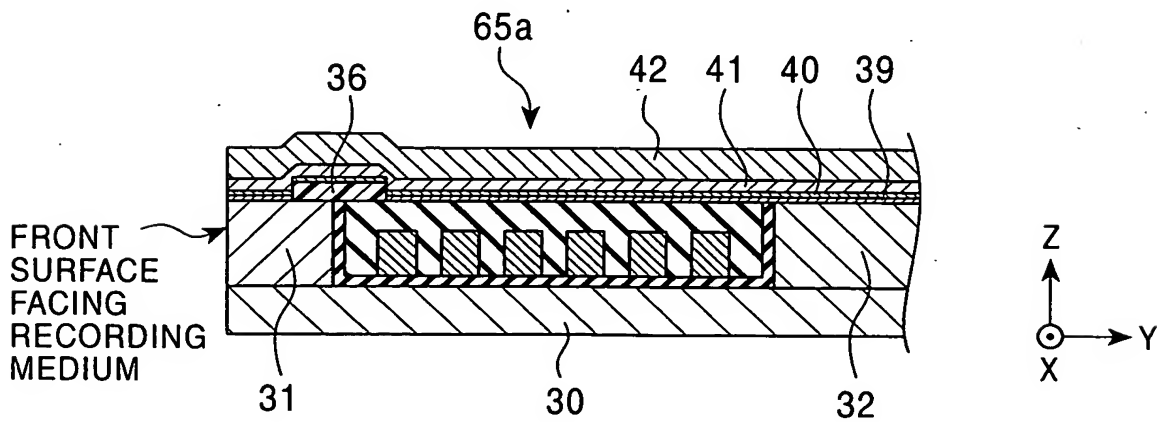




FIG. 17

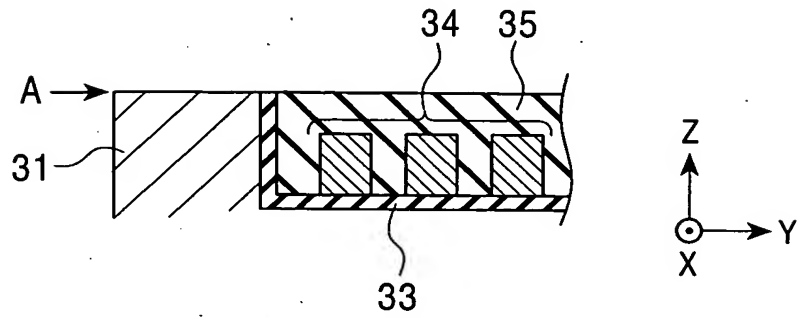


FIG. 18

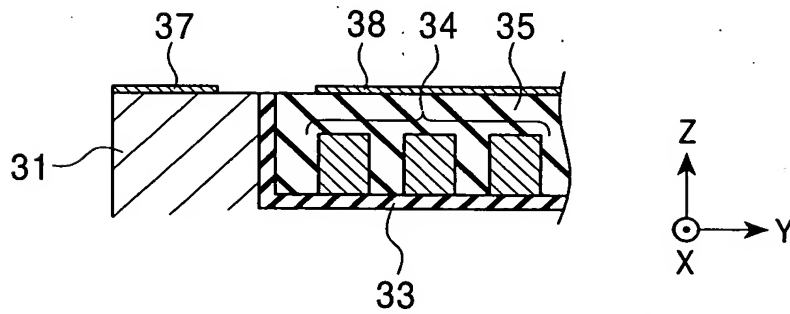
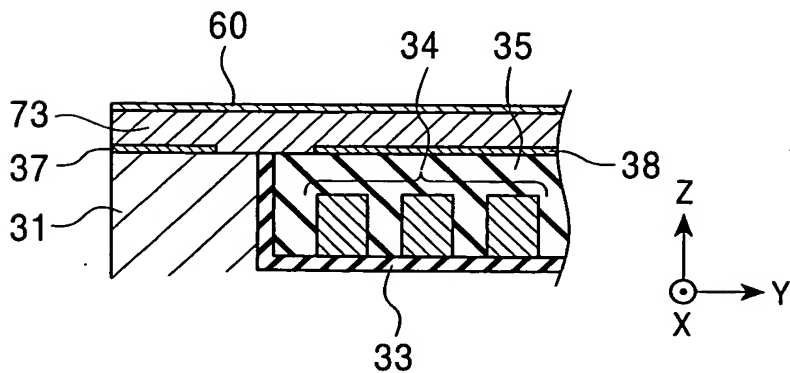


FIG. 19



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FIG. 20

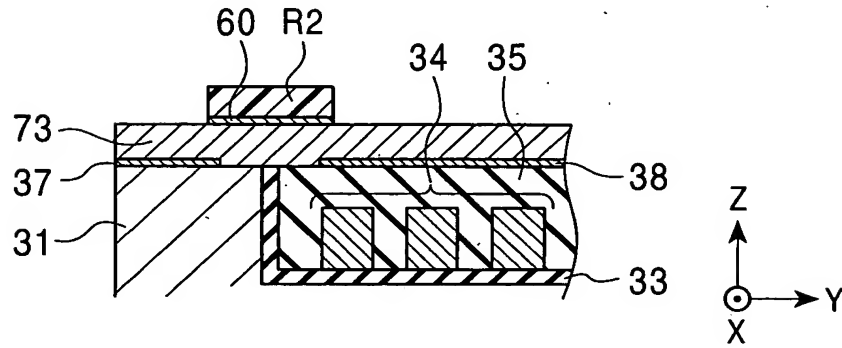


FIG. 21

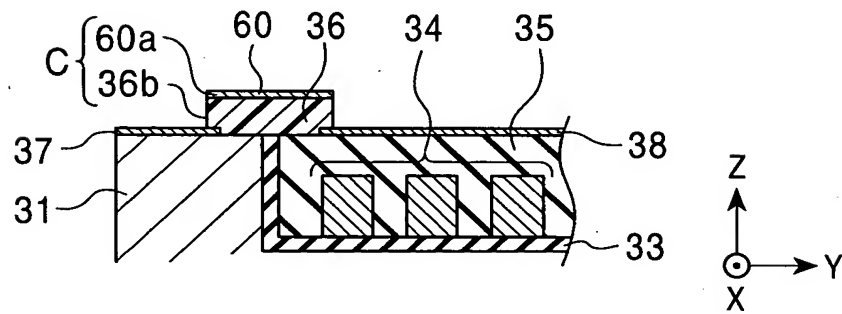


FIG. 22

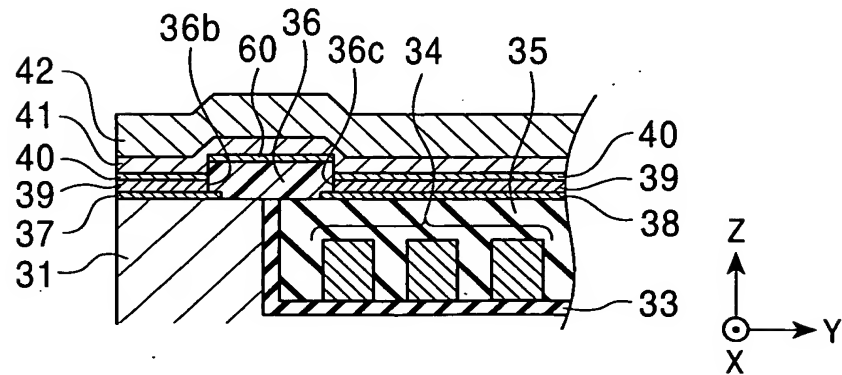


Fig. 1 is a cross-sectional view of a semiconductor device. It shows a substrate 31 with a top layer 37. A central region 34 contains three vertical structures 35. A top layer 38 covers the central region. A side layer 36 is on the left, and a bottom layer 33 is at the base. A coordinate system (X, Y, Z) is shown on the right.

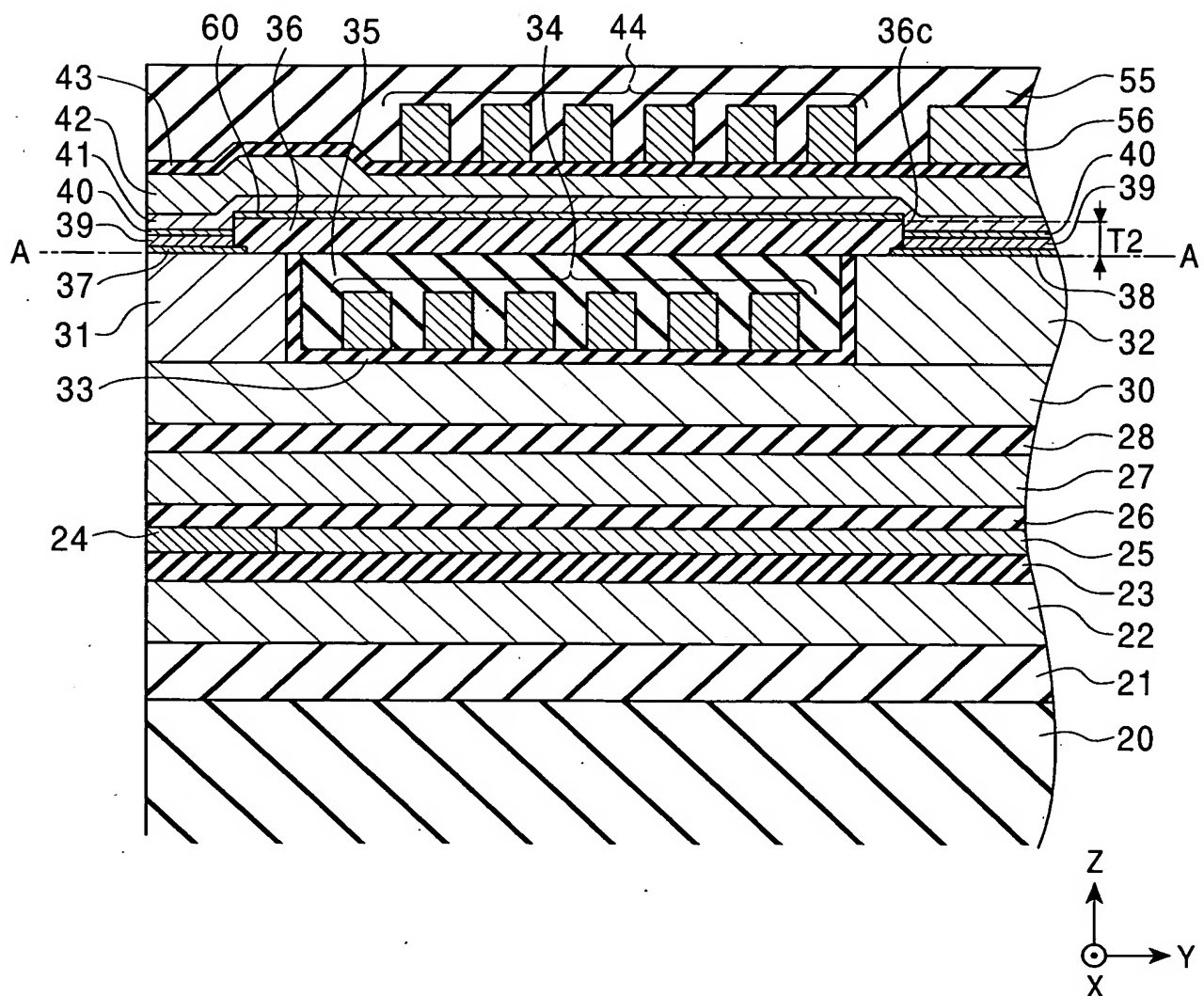
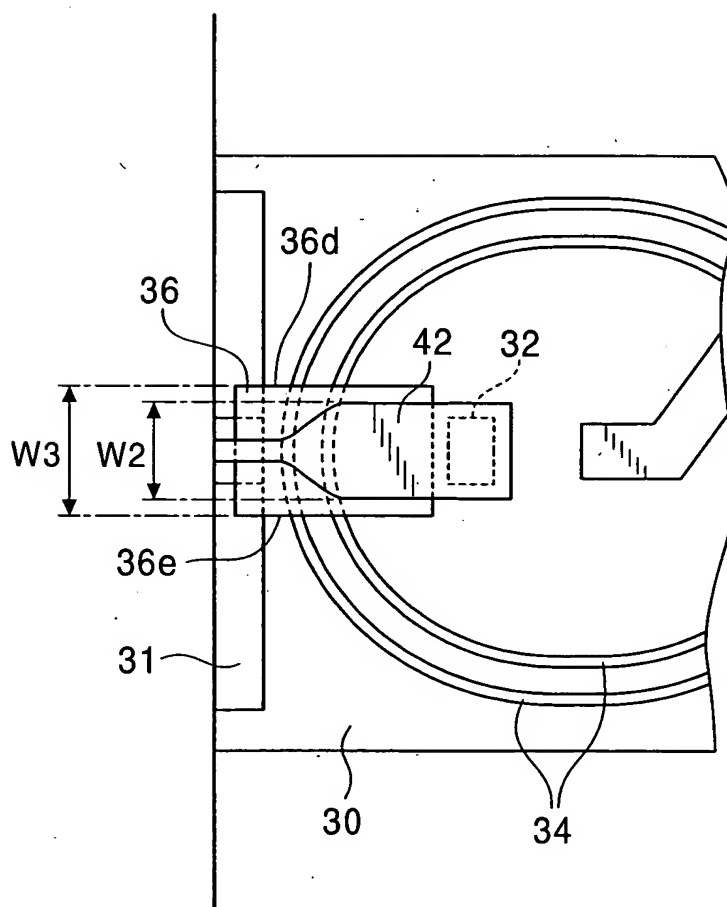


FIG. 26



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FIG. 27

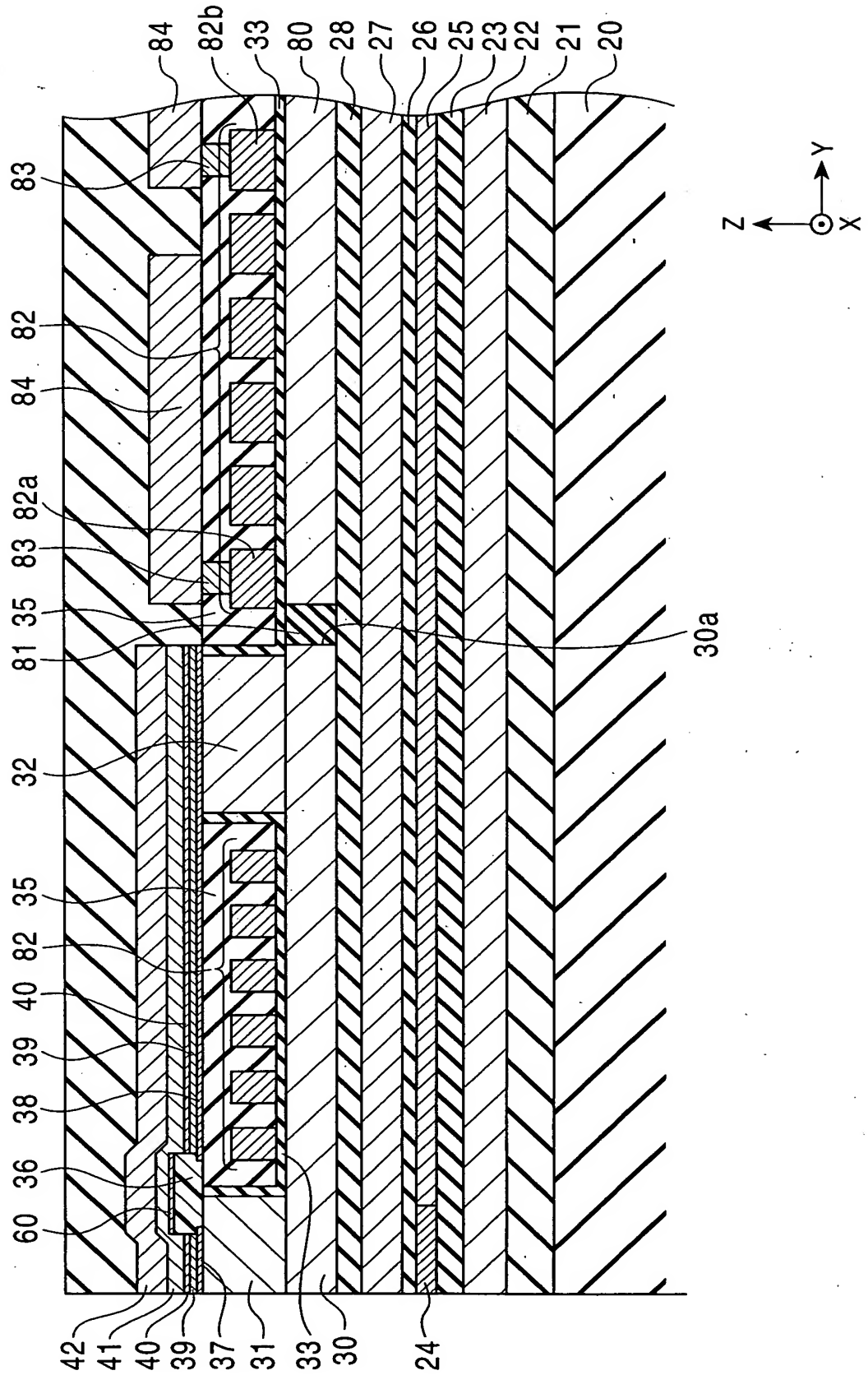


FIG. 28  
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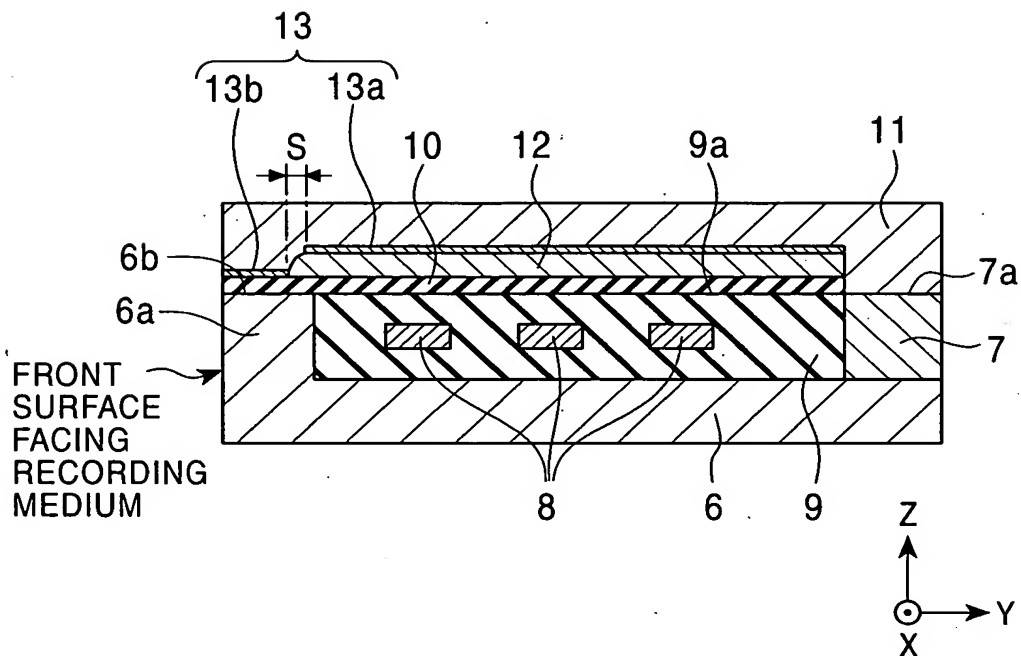


FIG. 29  
PRIOR ART

